

UNITED STATES DEI (TMENT OF COMMERCE Patent and Trademark Office

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FILING DATE

EXAMINER ART UNIT PAPER NUMBER DATE MAILED: 7/21/99

This is a communication from the examiner in charge of your application.

APPLICATION NUMBER

COMMISSIONER OF PATENTS AND TRADEMARKS OFFICE ACTION SUMMARY	
This action is FINAL.	
Since this application is in condition for allowance except for formal matters, pro accordance with the practice under <i>Ex parte Quayle</i> , 1935 D.C. 11; 453 O.G. 21	secution as to the merits is closed in 3.
A shortened statutory period for response to this action is set to expire	month(s), or thirty days, d within the period for response will cause be obtained under the provisions of 37 CFR
Disposition of Claims	
Claim(s)	is/are pending in the application
Of the above, claim(s)	
Claim(s)	is/are allowed.
Slaim(s) _ (1)	is/are rejected.
Claim(s)	is/are objected to.
Claims	are subject to restriction or election requiremen
Application Papers	
See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.	
The drawing(s) filed on is/are	objected to by the Examiner.
The proposed drawing correction, filed on	is approved disapprove
The specification is objected to by the Examiner.	
The oath or declaration is objected to by the Examiner.	
Priority under 35 U.S.C. § 119	
Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119	(a)-(d).
All Some None of the CERTIFIED copies of the priority docume	ents have been
received.	
received in Application No. (Series Code/Senal Number)	
received in this national stage application from the International Bureau (PC	T Rule 17.2(a)).
*Certified copies not received:	
Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 1	19(e).
Attachment(s)	
Notice of Reference Cited, PTO-892	Dung C. Dinh
Information Disclosure Statement(s), PTO-1449, Paper No(s).	Primary Examiner
Interview Summary, PTO-413	215
Notice of Draftsperson's Patent Drawing Review, PTO-948	
Notice of Informal Patent Application, PTO-152	

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Part III DETAILED ACTION

The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-2, 4-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Thornton et al. US patent 5,408,614.

As per claim 1, Thornton teaches system comprising:

a computer having a processing unit, main memory, and local bus [PC];

a device [modem adapter], where in the device occupies an I/O slot [COM1 or COM2] that is accessible at a first set of address [col.10 lines 26-40], the device has address assignment in a first set of address differs from a standard address assignment of a register set for a UART corresponding to the I/O slot [col.11 lines 7-15];

operating system execute by the processing unit, wherein the operating system includes procedure for accessing a register set of a UART corresponding to the first communication port [col.9 lines 35-37, BIOS];

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a communication driver [col.9 lines 40-50, redirection software] executed by the processing unit, the communication driver comprising a UART emulation [col.10 line 55 to col.11 line 21] which response to an access by the procedure for accessing the register set of a UART converts the access as required for the address assignment of the device.

Thornton does not teach the device being coupled to the local bus and has register set with address assignment in the first communication port. It is known prior art to couple a device to Thornton device is coupled to the parallel port to the local bus. save occupancy of the limited card slots in the PC. It would have been obvious for one of ordinary skill in the art to have device coupled to the local bus because it would have direct connection to the control/address/data bus within the PC. The address assignment of the register set would have been a matter of design choice because the process of converting accesses to a standard UART to the format used by the device would work equally well. It would have been obvious for one of ordinary skill in the art to assign the device register set to the address of the communication port it is replacing because it would have saved system resource by not taking up another I/O address range.

As per claim 2, it is well known in the art to have ISA bus in the PC. It is inherent that the Thornton's PC would have ISA bus.

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As per claim 4, Thornton teaches a method for communication between a computer and a device having I/O interface which is differs from the I/O interface of a UART, comprising:

allocating in memory of the computer storage locations which correspond to registers com a UART [col.10 line 55 to col.11 line 21, it is apparent that the redirection software would have allocation storage for the modem status and the reformatted data];

transmitting information via the local bus between the I/O interface of the device and the allocated memory locations in memory [apparent from col.10 line 55 to col.11 line 21 - data FIFO, UART status].

Thornton does not teach the device being coupled to the local bus. It is known prior art to couple a device to the local bus. Thornton device is coupled to the parallel port to save occupancy of the limited card slots in the PC. It would have been obvious for one of ordinary skill in the art to have device coupled to the local bus because it would have direct connection to the control/address/data bus within the PC.

As per claim 5, Thornton discloses transmitting from an application data packet formatted for a UART [col.8 lines 51-66]. It is apparent that the redirection software would update value in its storage locations.

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As per claim 6, Thornton teaches converting to value compatible with the interface and writing to register of the device [col.10 line 62-68].

As per claim 7, Thornton teaches reading from register of the device and updating storage location [col.11 lines 5-15, UART status data].

As per claim 8, it is apparent that the data would be transmit to the application.

As per claim 9, Thornton does not teach the device being assigned address allocated for UARTS. The address assignment would have been a matter of design choice because the process of converting accesses to a standard UART to the format used by the device would work equally well at different addresses. It would have been obvious for one of ordinary skill in the art to assign the device to the address of the UART it is replacing because it would have saved system resource by not taking up another I/O address range.

Claims 1,3, 4,9-10 are rejected under 35 U.S.C. 103(e) as being unpatentable over Gibson et al. US patent 5,640,594 in further view of Thornton et al. US patent 5,408,614.

As per claim 1, Gibson teaches a system comprising a computer with processing unit, memory, local bus and device coupled to the local bus occupying I/O slot, and operating system including

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procedure for accessing a register set of a UART corresponding to a first communication port[inherent in a PC].

Gibson does not teach the device with register set assignment in the communication port different than a standard assignment of a UART, communication driver to emulate a UART that converts UART accesses to the registers sets of the device.

Thornton teaches system comprising:

a device [modem adapter], where in the device occupies an I/O slot [COM1 or COM2] that corresponds to a first communication port [col.10 lines 26-40], the device has register set differs from a standard address assignment of a register set for a UART corresponding to the first communication port [col.11 lines 7-15];

operating system execute by the processing unit, wherein the operating system includes procedure for accessing a register set of a UART corresponding to the first communication port [col.9 lines 35-37, BIOS];

a communication driver [col.9 lines 40-50, redirection software] executed by the processing unit, the communication driver comprising a UART emulation [col.10 line 55 to col.11 line 21] which response to an access by the procedure for accessing the register set of a UART converts the access as required for register set and address assignment of the device.

Thornton does not teach the device being coupled to the local bus and has register set with address assignment in the first

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communication port. It is known prior art to couple a device to the local bus. Thornton device is coupled to the parallel port to save occupancy of the limited card slots in the PC. It would have been obvious for one of ordinary skill in the art to have device coupled to the local bus because it would have direct connection to the control/address/data bus within the PC. The address assignment of the register set would have been a matter of design choice because the process of converting accesses to a standard UART to the format used by the device would work equally well. It would have been obvious for one of ordinary skill in the art to assign the device register set to the address of the communication port it is replacing because it would have saved system resource by not taking up another I/O address range.

It would have been obvious for one of ordinary skill in the art to use Thornton teaching in Gibson system because it would have enable non-standard modem device to work with software designed to communicate with a standard UART [col.9 lines 57-66].

As per claim 3, Gibson suggested the device coupled to the local bus comprising:

- a comparator [fig.4A #312];
- a pattern generator [fig.4A SEQ(count)] coupled to the comparator;

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a counter [fig.4A COUNT] operable couple to the comparator and the pattern generator;

a register [fig.4B #324 accept data for device programming] coupled to the counter to receive signal from the local bus in respond to the counter reaching a final state [fig.4A #316].

As per claim 4, it is rejected under similar rationales as for claim 1 above.

As per claim 9, it is well known that the PC has I/O slots for UARTs. The reference do not teach setting the base address for the device at one of the I/O slot. It would have been obvious for one of ordinary skill in the art to assign the device register set to the address of the communication port it is replacing because it would have saved system resource by not taking up another I/O address range.

As per claim 10, it is rejected under similar rationale as for claim 3 above.

Claims 1 and 4 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 5,787,305. Although the conflicting claims are not identical, they are not patentably distinct from each other because the claims recited essentially

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identical elements performing the essentially same functions as claim 1 of U.S. Patent No. 5,787,305.

The non-statutory double patenting rejection, whether of the obviousness-type or non-obviousness-type, is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985) In re Van Ornum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); In re Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and In re Thorington, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a non-statutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dung Dinh whose telephone number is $(703)\ 305-9655$. The examiner can normally be reached on Monday-Thursday from $7:00\ AM-4:30\ PM$. The examiner can also be reached on alternate Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached at (703) 305-9717.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-9600.

Any response to this final action should be mailed to:

Box AF

Commissioner of Patents and Trademarks Washington, DC 20231

or faxed to:

(703) 308-9051, (for formal communications; please mark "EXPEDITED PROCEDURE")

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(703) 308-5359 (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

Dung Dinh

Patent Examiner August 20, 1997 -10-